

**IN THE TITLE**

Applicants note the filing of an Amendment herein on May 25, 2007 in which the title of the invention was amended to read:

**METHODS FOR FORMING A METALLIC DAMASCENE STRUCTURE**

and note that the amended title is not reflected in the Notice of Allowance and Fees Due dated August 13, 2007. Applicants respectfully request that the amended title be made of record herein.

IN THE SPECIFICATION:

Please amend paragraph [0005] as follows:

[0005] FIGS. 1A-1C illustrate a sequence of fabrication steps for a known dual damascene process as applied to interconnect formation. As shown in FIG. 1A, the process begins with the deposition of a first insulating layer 140 over a first level interconnect metal layer 120, which in turn is formed over or within a semiconductor substrate 100. A second insulating layer 160 is next formed over the first insulating layer 140. Etch stop layers 150, 150' are typically formed between the first and second insulating layers 140, 160 and between the first insulating layer 140 and the first level interconnect metal layer 120. The second insulating layer 160 is patterned by photolithography with a first mask (not shown) to form a trench 170 corresponding to a metal line of a second level interconnect. The etch stop layer 150 prevents the upper level trench ~~pattern~~ 170 from being etched through to the first insulating layer 140.

Please amend paragraph [0032] as follows:

[0032] ~~FIGS-FIGS.~~ 2H-2K are cross-sectional views illustrating a sequence of fabrication steps of an alternative embodiment of the invention;

Please amend paragraph [0065] as follows:

[0065] According to the teachings of the present invention, the selective deposition of copper by CVD described above is not the only method that can be employed for depositing the conductive material 280. According to another embodiment of the invention, copper can be selectively deposited by an electroless plating technique. In some ~~instance~~ instances, an electroless plating technique is more attractive than conventional electroplating methods. For example, in some embodiments, electroless plating is more advantageous than electroplating because of the low cost of tools and materials. An example of a study for electroless plating is provided in an article by Shacham-Diamand et al., entitled "Copper Electroless Deposition Technology for Ultra-Large-Scale -Integration (ULSI) Metallization," Microelectronic Engineering, Vol. 33, pp. 47-48 (1997), the disclosure of which is incorporated by reference

herein. As will be understood by one of ordinary skill in the art upon reading this disclosure, electroless plating has a very high selectivity, excellent step coverage and good via/trench filling because of the very thin seed layers formed by the electroless plating method.